REMARKS

Applicant appreciates the Examiner's attention to the above referenced application. Claims 1-20 were rejected. Claims 1, 2, 4, 5, 7, 9, 12, 13, 15, 17, 18 and 20 have been amended. Claims 1-20 are now pending, of which claims 1, 6, 12 and 17 are independent.

35 USC § 112 Rejection of the Claims

Claims 7 and 9-10 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claims 7 and 9 in response to this rejection, and respectfully requests that claims 7 and 9-10 be allowed to pass to issuance.

35 USC § 101 Rejection of the Claims

Claims 1-20 were rejected under 35 USC § 101 as being not limited to tangible embodiments. Applicant has amended claims 1, 12, and 20 in response to this rejection, and respectfully requests that claims 1-20 be allowed to pass to issuance.

35 USC § 102 Rejection of the Claims

Claims 1-5 were rejected under 35 USC § 102(b) as being anticipated by Sokolov et al. (US Publication No. 2004/0015873). Applicant has amended claims 1, 2, 4, and 5 and respectfully submits that claims 1-5 are in condition for allowance. Applicant respectfully requests that claims 1-5 be allowed to pass to issuance.

Claims 6-11 were rejected under 35 USC § 102(b) as being anticipated by Adl-Tabatabai et al. (US Patent No. 6,317,869). Applicant respectfully traverses this rejection, which should be withdrawn for at least the reasons set forth herein.

Independent claim 6 is repeated below:

6. A method for managing type information for operands, the method comprising:

shifting a bit value of 1 into a register, in conjunction with creation of a reference operand; and

shifting a bit value of 0 into the register, in conjunction with creation of a non-reference operand.

The Office Action states on pages 6-7 that "shifting a bit value [of 1 or 0] into a register" is taught by Adl-Tabatabai in Figs. 4b and 5b element 555 and columns 6 lines 39-56. Adl-Tabatabai describes a bit vector with "bits indicating the state of ... [corresponding] variables, where "a bit is set when the corresponding variable contains a reference type" and "when the corresponding variable does not contain a reference type, then the bit is cleared." (See Adl-Tabatabai, column 6, lines 8-16.) The Office Action further explains that "shifting can be defined as switching or exchange of. Thus, the replacement of data in the bit vector with a bit value of 1 is shifting." Applicants respectfully disagree. One of skill in the art understands that shifting a bit value into a register performs an arithmetic operation on the contents of the register, thereby replacing the contents of the register with a different value. The values of all bits in the register may be affected by the shift operation. The setting of a single bit within a vector does not affect other bits within the vector, and thus Adl-Tabatabai does not teach "shifting a bit value [of 1 or 0] into a register." Claim 6 and its dependent claims 7-11 are allowable for at least this reason.

The Office Action further points out that Adl-Tabatabai indicates that "the bit vector may be stored in registers." (See Adl-Tabatabai, lines 26-27.) Even if Adl-Tabatabai's bit vector were stored in registers, the changing of a single value of a bit within the bit vector does not teach shifting a particular bit value into the register to perform the arithmetic operation described above. Claim 6 and its dependent claims 7-11 are allowable for at least this reason.

Claim 7 further includes the limitation:

initializing the tag stack register by:

assigning a low order bit of the tag stack register to a value of 0; and

assigning other bits of the tag stack register to a value of 1.

The Office Action states that this limitation is taught in column 6 lines 8-16, quoted above, which merely teach changing a single bit value within a bit vector. Initialization of the bit

vector is not discussed and would be irrelevant, since operations are performed only on single bits within the bit vector and not on the bit vector as a whole. In contrast, initialization of the low order bit of the register to a value of 0 and other bits in the register to a value of 1 affects the contents of the register and enables the register to perform the arithmetic operation described above when a shift operation is performed.

Claims 6-11 are allowable for at least the foregoing reasons, and Applicants respectfully request that claims 6-11 be allowed to pass to issuance.

35 USC § 103 Rejection of the Claims

Claims 12-20 were rejected under 35 USC § 103(a) as being unpatentable over Sokolov et al. (US Publication No. 2004/0015873). Applicant has amended claims 12, 13, 15, 17, 18, and 20, and respectfully submits that claims 12-20 are in condition for allowance. Applicant respectfully requests that claims 12-20 be allowed to pass to issuance.

CONCLUSION

Applicant respectfully requests reconsideration in view of the remarks and amendments set forth above. If the Examiner has any questions, the Examiner is encouraged to contact the undersigned at (512) 732-1303. Please charge any shortage of fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 50-0221 and please credit any excess fees to such account.

Respectfully submitted,

Customer No. 59796

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/D'Ann Naylor Rifai/
D'Ann Naylor Rifai
Reg. No. 47,026
Patent Attorney
Intel Corporation
(512) 732-1303